ABSTRACT OF THE DISCLOSURE

A parallel/serial conversion circuit is provided, which comprises a parallel/serial conversion section for converting first parallel data to first serial data and converting second parallel data to second serial data, and a shift clock signal generation section for generating a shift clock signal. The parallel/serial conversion section converts the first parallel data to the first serial data by shifting the first parallel data in response to the shift clock signal. The parallel/serial conversion section converts the second parallel data to the second serial data by shifting the second parallel data in response to the shift clock signal. A combination of the first serial data and the second serial data indicates bit separation, a logic value '0', or a logic value '1'. The shift clock signal generation section generates the shift clock signal by combining the first serial data and the second serial data.